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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,057	04/21/2004	Charles Norman Shaver	200314194-1	5954

22879 7590 06/16/2006

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EXAMINER

SPITTLE, MATTHEW D

ART UNIT PAPER NUMBER

2111

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/829,057	Applicant(s) SHAVER ET AL.	
	Examiner Matthew D. Spittle	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-11 and 13-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-11 and 13-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1, 2, 4 – 11, and 13 – 18 have been examined.

Allowable Subject Matter

The indicated allowability of claims 1, 2, 4 – 11, and 13 – 18 is withdrawn in view of the newly discovered reference(s) to Henrie. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 9 recites the limitation "the internal USB port" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 4, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henrie.

Regarding claim 1, Henrie teaches a system for providing Universal Serial Bus (USB) having a first USB header (column 5, lines 4 – 6; Examiner interprets the connecting port on the host computer as the first USB header) for communicating with an external USB port (Figure 1a, item 18 – USB PORT 7), said system comprising:

A printed wire board (PWB) (Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to implement a circuit as shown in Figures 1a, on a printed wired board.) supporting a second USB header (Figure 1a, item 12 – USB PORT 0; column 5, lines 4 – 6), a third USB header (Figure 1a, item 18 – USB PORT 7), a USB hub (Figure 1a, item 10).

The second USB header (Figure 1a, item 18 – USB PORT 0) operative to communicate with the first USB header (column 5, lines 4 – 6 teach that the second USB header (PORT 0) is connected to the first USB header located on the host computer);

The third USB header operative to communicate with the external USB port (Figure 1a, item 18 – USB PORT 7; column 1, lines 31 – 33);

The USB hub (Figure 1a, item 10) operative to communicate information to and from the first USB header of the motherboard via the second USB header (Figure 1a,

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item 12 – USB PORT 0), and to communicate information to and from the external USB port via the third USB header (Examiner interprets the third USB header comprising the external USB port (Figure 1a, item 18 – USB PORT 7), and all connected wiring as shown in Figure 5 (See pins 4 and 5 of the USB CONTROLLER (10)).

A voltage regular supported by the PWB, the voltage regulator being operative to receive a first voltage output from the motherboard and to provide, in response thereto, a second, lower voltage output to the USB hub (Figure 1a, item 14; Figure 7).

Henrie implicitly teaches the limitation of the computer chassis internally mounting a motherboard and having a first USB header since he teaches a host computer having USB ports (Figure 9B, item 68), and computers are well known to have motherboards containing USB ports as evidenced by Nouzovsky et al. (Figure 1, items 10, 14, 18).

Henrie fails to teach an internal USB port being operative to communicate information to and from the motherboard via the USB hub. Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the external ports (Figure 1a, item 18) could serve as internal USB ports and thereby support internal USB devices. Additionally, this configuration could still support external USB devices simply by routing the USB cable from the hub through an unused card slot on the back of the computer chassis to the external device.

Henrie fails to teach the PWB being mountable at a location within the computer chassis. Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to provide a mounting means for any

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component located within the computer chassis. The motivation for doing this would be to prevent damage from occurring during movement (such as in transportation) of the computer chassis due to the component physically impacting other components of the computer.

Regarding claim 2, Henrie teaches the additional limitation wherein the location at which the PWB is mounted is a location other than a Peripheral Component Interface (PCI) expansion slot of the computer chassis (Examiner notes that the PWB of Henrie does not require a PCI expansion slot).

Regarding claim 4, Henrie teaches the additional limitation wherein the first voltage output is approximately 5 volts, and the second voltage output is approximately 3.3 volts (Figure 7).

Regarding claim 5, Henrie teaches the additional limitation wherein the PWB is operative to receive a third voltage output from the motherboard, the third voltage output being routed by the PWB to power the external USB port (Figure 1a, item 18; column 5, line 62 – column 6, line 5; where VBUSIN is provided by the motherboard in the host computer).

Regarding claim 8, Henrie teaches the additional limitation of a first USB cable operative to interconnect the first USB header of the motherboard with the second USB

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header (as exemplified in Figure 9B where USB PORT0 may be interpreted as the second USB header and USB PORT2 may be interpreted as the first USB header of the motherboard);

Henrie fails to explicitly teach a second USB cable operative to interconnect the third USB header with the external USB port. Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to attach a USB extension cable to a port of the USB hub (interpreted as a third USB header; Figure 1a, item 18) inside of the computer chassis and route the cable through an unused card slot on the back of the computer chassis to provide an "external" USB port from the internal third USB header.

* * *

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henrie in view of Le et al.

Regarding claim 6, Henrie teaches a system for providing an internal Universal Serial Bus (USB) port within a computer chassis, the computer chassis internally mounting a motherboard having a first USB header for communicating with an external USB port, said system comprising:

A printed wire board (PWB) (Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to implement a circuit as shown in Figures 1a, on a printed wired board.) supporting a

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second USB header (Figure 1a, item 12 – USB PORT 0; column 5, lines 4 – 6), a third USB header (Figure 1a, item 18 – USB PORT 7), a USB hub (Figure 1a, item 10).

The second USB header (Figure 1a, item 18 – USB PORT 0) operative to communicate with the first USB header (column 5, lines 4 – 6 teach that the second USB header (PORT 0) is connected to the first USB header located on the host computer);

The third USB header operative to communicate with the external USB port (Figure 1a, item 18 – USB PORT 7; column 1, lines 31 – 33);

The USB hub (Figure 1a, item 10) operative to communicate information to and from the first USB header of the motherboard via the second USB header (Figure 1a, item 12 – USB PORT 0), and to communicate information to and from the external USB port via the third USB header (Examiner interprets the third USB header comprising the external USB port (Figure 1a, item 18 – USB PORT 7), and all connected wiring as shown in Figure 5 (See pins 4 and 5 of the USB CONTROLLER (10)).

Henrie implicitly teaches the limitation of the computer chassis internally mounting a motherboard and having a first USB header since he teaches a host computer having USB ports (Figure 9B, item 68), and computers are well known to have motherboards containing USB ports as evidenced by Nouzovsky et al. (Figure 1, items 10, 14, 18).

Henrie fails to teach an internal USB port being operative to communicate information to and from the motherboard via the USB hub. Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the

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external ports (Figure 1a, item 18) could serve as internal USB ports and thereby support internal USB devices. Additionally, this configuration could still support external USB devices simply by routing the USB cable from the hub through an unused card slot on the back of the computer chassis to the external device.

Henrie fails to teach the chassis having mounts extending into the interior thereof and the PWB having apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into the apertures secures the PWB to the chassis.

Le et al. teach the chassis (Figures 3A, 3B, item 100) having mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The PWB has apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into the apertures secures the PWB to the chassis (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the mounting means as taught by Le et al. into the system of Lelong et al. for the purpose of mounting the PWB in a secure manner to the chassis to prevent damage from occurring due to the PWB physically impacting the other components.

Regarding claim 7, Le et al. teach the additional limitation wherein the mounts form interference fits with the apertures when the mounts are inserted within the

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apertures (Figure 3A and 3B clearly show an interference fit between the mounts (items 333, 334) and the apertures (item 221)).

* * *

Claims 9, 10, 11, 13, 14, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henrie.

Regarding claim 9, Henrie teaches a computer system comprising:

A chassis defining an interior (Figure 9b, item 68; where a computer inherently comprises a chassis defining an interior);

A first Universal Serial Bus (USB) port externally mounted to the chassis (Figure 9b, item USB PORT2);

A motherboard mounted within the interior of the chassis, the motherboard having a first USB header for communicating with the first USB port (Henrie implicitly teaches the limitation of the computer chassis internally mounting a motherboard and having a first USB header since he teaches a host computer having USB ports (Figure 9B, item 68), and computers are well known to have motherboards containing USB ports as evidenced by Nouzovsky et al. (Figure 1, items 10, 14, 18). Examiner notes that the USB port (18) as shown in Figure 1 appears to be mounted externally to the chassis.);

A daughter card mounted within the interior of the chassis (Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of

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invention by applicant to implement the circuit of Figure 1a in a daughter card or printed circuit/wire board of any type; Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the external ports (Figure 1a, item 18) could serve as internal USB ports and thereby support internal USB devices), the daughter card communicating with the motherboard and having a second USB port (Figure 1a, item 18 – USB PORT 1), a USB hub (Figure 1a, item 10), a second USB header (Figure 1a, item 18 – USB PORT 0), and a third USB header (Figure 1a, item 18 – USB PORT 7; column 1, lines 31 – 33);

The USB hub (Figure 1a, item 10) operative to communicate information to and from the first USB header of the motherboard via the second USB header (Figure 1a, item 12 – USB PORT 0), and to communicate information to and from the external USB port via the third USB header (Examiner interprets the third USB header comprising the external USB port (Figure 1a, item 18 – USB PORT 7), and all connected wiring as shown in Figure 5 (See pins 4 and 5 of the USB CONTROLLER (10)).

A voltage regular supported by the daughter card, the voltage regulator being operative to receive a first voltage output from the motherboard and to provide, in response thereto, a second, lower voltage output to the USB hub (Figure 1a, item 14; Figure 7).

Henrie fails to teach an internal USB port being operative to communicate information to and from the motherboard via the USB hub. Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the external ports (Figure 1a, item 18) could serve as internal USB ports and thereby

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support internal USB devices. Additionally, this configuration could still support external USB devices simply by routing the USB cable from the hub through an unused card slot on the back of the computer chassis to the external device.

Regarding claim 10, Henrie teaches the additional limitation wherein the location at which the daughter card is mounted is a location other than a Peripheral Component Interface (PCI) expansion slot of the computer chassis (Examiner notes that the daughter card of Henrie does not require a PCI expansion slot).

Regarding claim 11, Henrie implicitly teaches the additional limitation wherein the motherboard controls continuity of power to the daughter card (Examiner notes that in Figure 1a, the daughter card (5) receives power from VBUSIN, which comes from host computer (column 5, lines 4 – 15; column 5, line 62 – column 6, line 5), which inherently contains a motherboard and therefore meets this limitation).

Regarding claim 13, Henrie teaches the additional limitation wherein the first voltage output is approximately 5 volts, and the second voltage output is approximately 3.3 volts (Figure 7).

Regarding claim 14, Henrie teaches the additional limitation wherein the PWB is operative to receive a third voltage output from the motherboard, the third voltage output being routed by the daughter card to power the external USB port (Figure 1a, item 18;

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column 5, line 62 – column 6, line 5; where VBUSIN is provided by the motherboard in the host computer).

Regarding claim 15, Henrie fails to teach means for securing the daughter card to the chassis. Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to provide a mounting means for any component located within the computer chassis. The motivation for doing this would be to prevent damage from occurring during movement (such as in transportation) of the computer chassis due to the component physically impacting other components of the computer.

Regarding claim 18, Henrie teaches the additional limitation of a first USB cable operative to interconnect the first USB header of the motherboard with the second USB header (as exemplified in Figure 9B where USB PORT0 may be interpreted as the second USB header and USB PORT2 may be interpreted as the first USB header of the motherboard);

Henrie fails to explicitly teach a second USB cable operative to interconnect the third USB header with the external USB port. Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to attach a USB extension cable to a port of the USB hub (interpreted as a third USB header; Figure 1a, item 18) inside of the computer chassis and route the cable through

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an unused card slot on the back of the computer chassis to provide an "external" USB port from the internal third USB header.

* * *

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henrie.

*Regarding claim 16, Henrie teaches a computer system comprising:

A chassis defining an interior (Figure 9b, item 68; where a computer inherently comprises a chassis defining an interior);

A first Universal Serial Bus (USB) port externally mounted to the chassis (Figure 9b, item USB PORT2);

A motherboard mounted within the interior of the chassis, the motherboard having a first USB header for communicating with the first USB port (Henrie implicitly teaches the limitation of the computer chassis internally mounting a motherboard and having a first USB header since he teaches a host computer having USB ports (Figure 9B, item 68), and computers are well known to have motherboards containing USB ports as evidenced by Nouzovsky et al. (Figure 1, items 10, 14, 18). Examiner notes that the USB port (18) as shown in Figure 1 appears to be mounted externally to the chassis.);

A daughter card mounted within the interior of the chassis (Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of

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invention by applicant to implement the circuit of Figure 1a in a daughter card or printed circuit/wire board of any type; Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the external ports (Figure 1a, item 18) could serve as internal USB ports and thereby support internal USB devices), the daughter card communicating with the motherboard and having a second USB port (Figure 1a, item 18 – USB PORT 1), a USB hub (Figure 1a, item 10), a second USB header (Figure 1a, item 18 – USB PORT 0), and a third USB header (Figure 1a, item 18 – USB PORT 7; column 1, lines 31 – 33);

The USB hub (Figure 1a, item 10) operative to communicate information to and from the first USB header of the motherboard via the second USB header (Figure 1a, item 12 – USB PORT 0), and to communicate information to and from the external USB port via the third USB header (Examiner interprets the third USB header comprising the external USB port (Figure 1a, item 18 – USB PORT 7), and all connected wiring as shown in Figure 5 (See pins 4 and 5 of the USB CONTROLLER (10)).

Henrie fails to teach an internal USB port being operative to communicate information to and from the motherboard via the USB hub. Examiner takes official notice that by moving the USB hub of Henrie to the inside of the computer chassis, the external ports (Figure 1a, item 18) could serve as internal USB ports and thereby support internal USB devices. Additionally, this configuration could still support external USB devices simply by routing the USB cable from the hub through an unused card slot on the back of the computer chassis to the external device.

Henrie fails to teach the chassis having mounts extending into the interior thereof and the PWB having apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into the apertures secures the PWB to the chassis.

Le et al. teach the chassis (Figures 3A, 3B, item 100) having mounts extending into the interior thereof (Figures 3A, 3B; items 333, 334);

The PWB has apertures formed therethrough, each of the apertures being operative to receive one of the mounts such that insertion of the mounts into the apertures secures the PWB to the chassis (where the PWB is interpreted in Figures 3A and 3B as item 220, and the apertures are interpreted as mounting holes (item 221)).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the mounting means as taught by Le et al. into the system of Lelong et al. for the purpose of mounting the PWB in a secure manner to the chassis to prevent damage from occurring due to the PWB physically impacting the other components.


Regarding claim 17, Le et al. teach the additional limitation wherein the mounts form interference fits with the apertures when the mounts are inserted within the apertures (Figure 3A and 3B clearly show an interference fit between the mounts (items 333, 334) and the apertures (item 221)).

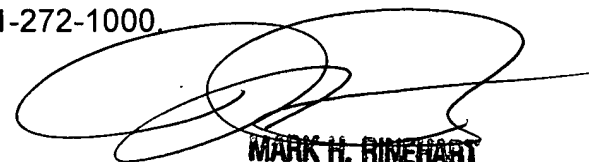
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


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